Electronic Version
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Claims

[c1] What is claimed is:

1.A pixel of a thin film transistor array substrate comprising:

a thin film transistor having a gate electrode comprising a first metallic layer, and source/drain electrodes comprising a second metallic layer;

a passivation layer positioned on the thin film transistor;

a photosensitive layer positioned on the passivation layer;

a reflective layer positioned on the light-sensitive layer; and

a light-shielding layer positioned below the photosensitive layer and beside the thin film transistor for preventing light beams from penetrating the light-shielding layer.

[c2] 2.The pixel of claim 1 wherein the light-shielding layer comprises the first metallic layer.

[c3] 3.The pixel of claim 1 wherein the light-shielding layer comprises the second metallic layer.

[c4] 4.The pixel of claim 1 wherein the light-shielding layer

comprises the first metallic layer and the second metallic layer.

[c5] 5.The pixel of claim 1 wherein the light-shielding layer comprises a multi-layer reflective film.

[c6] 6.The pixel of claim 1 wherein the thin film transistor array substrate is a semi-reflective thin film transistor array substrate.

[c7] 7.The pixel of claim 1 wherein the thin film transistor array substrate is a reflective thin film transistor array substrate.

[c8] 8.The pixel of claim 6 further comprising a pervious to light layer on the passivation layer, the pervious to light layer comprising ITO or IZO.

[c9] 9.The pixel of claim 8 wherein the pervious to light region and the light-shielding layer have an overlapping region where the pervious to light region partially overlaps with the light-shielding layer, and a ratio of a first area of the overlapping region to a second area of the pixel is between 0

and 15%.

[c10] 10.The pixel of claim 8 wherein the pervious to light re-

gion and the light-shielding layer have an overlapping region where the pervious to light region partially overlaps with the light-shielding layer, and a ratio of a first area of the overlapping region to a second area of the pixel is between

0 and 5%

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[c11] 11.The pixel of claim 1 wherein the light-shielding layer and the reflective layer have an overlapping region where the light-shielding layer partially overlaps with the reflective layer, and a ratio of a first area of the overlapping region to a second area of the reflective layer is between

30% and 100%.

[c12] 12.The pixel of claim 1 wherein the light-shielding layer and the reflective layer have an overlapping region where the light-shielding layer partially overlaps with the reflective layer, and a ratio of a first area of the overlapping region to a second area of the reflective layer is larger than

60%.

[c13] 13.The pixel of claim 1 wherein the reflective layer comprises aluminum, silver or an alloy comprising aluminum and silver.

[c14] 14.The pixel of claim 1 wherein the first metallic layer and the second metallic layer comprise aluminum, silver, chromium, molybdenum or an alloy comprising aluminum, silver, chromium and molybdenum.

[c15] 15.The pixel of claim 1 wherein the photosensitive layer comprises a positive photoresist material or a negative photoresist material.

[c16] 16.The pixel of claim 1 wherein the thin film transistor array substrate is an amorphous silicon thin film transistor array substrate.

[c17] 17.The pixel of claim 1 wherein the thin film transistor array substrate is a low temperature polysilicon thin film transistor array substrate.

[c18] 18.A method for forming a pixel of a thin film transistor array substrate comprising:
providing a substrate comprising a thin film transistor having a gate electrode comprising a first metallic layer and source/drain electrodes comprising a second metallic layer, a passivation layer formed on the thin film transistor, a photosensitive layer formed on the passivation

layer, and a light-shielding layer formed below the photosensitive layer and beside the thin film transistor;
utilizing the light-shielding layer to shelter from light beams generated in a photolithography process for preventing the light beams from penetrating the light-shielding layer; and
utilizing the light-shielding layer to reflect the light beams to irradiate the photosensitive layer again for reducing exposure time of the photolithography process.

[c19] 19.The method of claim 18 wherein the light-shielding layer comprises the first metallic layer.

[c20] 20.The method of claim 18 wherein the light-shielding layer comprises the second metallic layer.

[c21] 21.The method of claim 18 wherein the light-shielding layer comprises both the first metallic layer and the second metallic layer.

[c22] 22.The method of claim 16 further comprising forming a pervious to light layer composed of ITO or IZO on the passivation layer.

[c23] 23.The method of claim 22 wherein the pervious to light region and the light-shielding layer have an overlapping region where the pervious to light region partially overlaps with the light-shielding layer, and a ratio of an area

of the overlapping region to an area of the pixel is between

0 and 5%

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[c24] 24.The method of claim 21 wherein the pervious to light region and the light-shielding layer have an overlapping region where the pervious to light region partially overlaps with the light-shielding layer, and a ratio of an area of the overlapping region to an area of the pixel is between

0 and 5%

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[c25] 25.The method of claim 18 wherein the light-shielding layer and the reflective layer have an overlapping region where the light-shielding layer partially overlaps with the reflective layer, and a ratio of an area of the overlapping region to an area of the reflective layer is between

30% and 100%.

[c26] 26.The method of claim 18 wherein the light-shielding layer and the reflective layer have an overlapping region where the light-shielding layer partially overlaps with the

reflective layer, and a ratio of an area of the overlapping region to an area of the reflective layer is larger than 60%.